IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A phase-locked loop (PLL) frequency synthesizer comprising:

a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency, Fout, determined by said frequency control voltage level;

a first frequency divider for dividing said operating frequency, Fout, of said output clock signal by a first divider value, N, to produce a first divided clock signal having a frequency, Fout/N;

a second frequency divider for dividing a reference frequency, Fin, of an incoming reference clock signal by a second divider value, M, to produce a second divided clock signal having a frequency, Fin/M;

a phase-frequency detector capable of comparing said first and second divided clock signals and generating an UP control signal if said first divided clock signal is slower than said second divided clock signal and generating a DOWN control signal if said first divided clock signal is faster than said second divided clock signal;

a charge pump capable of receiving said UP and DOWN control signals and increasing said frequency control voltage level on said loop filter by injecting a charge pump current, Ic,

and decreasing said frequency control voltage level on said loop filter by draining said charge pump current, Ic; and

a loop response control circuit capable of adjusting a value of Ic as a function of said first divider value, N, and said second divider value, M, wherein said loop response control circuit is capable of adjusting the value of Ic based at least partially on at least one of a range in which said first divider value lies and a range in which said second divider value lies.

2. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 1 wherein said loop response control circuit, for a given value of M, sets Ic to a minimum current level when N is in the range $1 \leq N \leq K$ and sets Ic to a second current level higher than said minimum current level when N is in the range $K+1 \leq N \leq P$.

3. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 2 wherein said second current level is approximately twice said minimum current level.

4. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 3 wherein said loop response control circuit sets Ic to a third current level higher than said second current level when N is in the range $P+1 \leq N \leq S$.

5. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 4 wherein said third current level is approximately twice said second current level.

6. (Currently Amended) The phase-locked loop frequency synthesizer as set forth in Claim 1 wherein said loop response control circuit, for a given value of N, sets Ic to a maximum current level when M is in the range $1 \leq M \leq J$ and sets Ic to a second current level lower than said maximum current level when M is in the range $K+1 \leq ~~N~~ \underline{M} \leq Q$.

7. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 6 wherein said second current level is approximately one half of said maximum current level.

8. (Currently Amended) The phase-locked loop frequency synthesizer as set forth in Claim 7 wherein said loop response control circuit sets Ic to a third current level lower than said second current level when M is in the range $Q+1 \leq ~~N~~ \underline{M} \leq T$.

9. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 8 wherein said third current level is approximately one half of said second current level.

10. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 1 wherein said loop response control circuit is further capable of adjusting a resistance, R, of a filter resistor associated with said loop filter as a function of said first divider value, N, and said second divider value, M.

11. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 10 wherein said loop response control circuit, for a given value of N, sets R to a minimum resistance value when M is in the range $1 \leq M \leq U$ and sets R to a second resistance level higher than said minimum resistance level when M is in the range $U+1 \leq M \leq V$.

12. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 11 wherein said second resistance level is approximately twice said minimum resistance level.

13. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 12 wherein said loop response control circuit sets R to a third resistance level higher than said second resistance level when M is in the range $V+1 \leq M \leq W$.

14. (Original) The phase-locked loop frequency synthesizer as set forth in Claim 13 wherein said third resistance level is approximately twice said second resistance level.

15. (Currently Amended) An integrated circuit comprising:

a processor capable of operating at a plurality of clock speeds;

a phase-locked loop (PLL) frequency synthesizer capable of providing at least one clock signal having a variable clock speed to said processor, said PLL frequency synthesizer comprising:

a voltage controlled oscillator (VCO) that receives a frequency control voltage level stored on a loop filter and generates an output clock signal having an operating frequency, Fout, determined by said frequency control voltage level;

a first frequency divider for dividing said operating frequency, Fout, of said output clock signal by a first divider value, N, to produce a first divided clock signal having a frequency, Fout/N;

a second frequency divider for dividing a reference frequency, Fin, of an incoming reference clock signal by a second divider value, M, to produce a second divided clock signal having a frequency, Fin/M;

a phase-frequency detector capable of comparing said first and second divided clock signals and generating an UP control signal if said first divided clock signal is slower than said second divided clock signal and generating a DOWN control signal if said first divided clock signal is faster than said second divided clock signal;

a charge pump capable of receiving said UP and DOWN control signals and increasing said frequency control voltage level on said loop filter by injecting a charge

pump current, Ic, and decreasing said frequency control voltage level on said loop filter by draining said charge pump current, Ic; and

a loop response control circuit capable of adjusting a value of Ic as a function of said first divider value, N, and said second divider value, M, wherein said loop response control circuit is capable of adjusting the value of Ic based at least partially on at least one of a range in which said first divider value lies and a range in which said second divider value lies.

16. (Original) The integrated circuit as set forth in Claim 15 wherein said loop response control circuit, for a given value of M, sets Ic to a minimum current level when N is in the range $1 \leq N \leq K$ and sets Ic to a second current level higher than said minimum current level when N is in the range $K+1 \leq N \leq P$.

17. (Original) The integrated circuit as set forth in Claim 16 wherein said second current level is approximately twice said minimum current level.

18. (Original) The integrated circuit as set forth in Claim 17 wherein said loop response control circuit sets Ic to a third current level higher than said second current level when N is in the range $P+1 \leq N \leq S$.

19. (Original) The integrated circuit as set forth in Claim 18 wherein said third current level is approximately twice said second current level.

20. (Currently Amended) The integrated circuit as set forth in Claim 15 wherein said loop response control circuit, for a given value of N, sets Ic to a maximum current level when M is in the range $1 \leq M \leq J$ and sets Ic to a second current level lower than said maximum current level when M is in the range $K+1 \leq ~~N~~ \underline{M} \leq Q$.

21. (Original) The integrated circuit as set forth in Claim 20 wherein said second current level is approximately one half of said maximum current level.

22. (Currently Amended) The integrated circuit as set forth in Claim 21 wherein said loop response control circuit sets Ic to a third current level lower than said second current level when M is in the range $Q+1 \leq ~~N~~ \underline{M} \leq T$.

23. (Original) The integrated circuit as set forth in Claim 22 wherein said third current level is approximately one half of said second current level.

24. (Original) The integrated circuit as set forth in Claim 15 wherein said loop response control circuit is further capable of adjusting a resistance, R, of a filter resistor associated with said loop filter as a function of said first divider value, N, and said second divider value, M.

25. (Original) The integrated circuit as set forth in Claim 24 wherein said loop response control circuit, for a given value of N, sets R to a minimum resistance value when M is in the range $1 \leq M \leq U$ and sets R to a second resistance level higher than said minimum resistance level when M is in the range $U+1 \leq M \leq V$.

26. (Original) The integrated circuit as set forth in Claim 25 wherein said second resistance level is approximately twice said minimum resistance level.

27. (Original) The integrated circuit as set forth in Claim 26 wherein said loop response control circuit sets R to a third resistance level higher than said second resistance level when M is in the range $V+1 \leq M \leq W$.

28. (Original) The integrated circuit as set forth in Claim 27 wherein said third resistance level is approximately twice said second resistance level.